[Total No. of Questions - 9] [Total No. of Printed Pages - 3]
(2125)

**15311**

**B. Tech 7th Semester Examination**

**Micro Electronics Technology (NS)**

**EC-411(a)**

**Time : 3 Hours** **Max. Marks : 100**

*The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.*

**Note :** (i) Attempt five questions in all selecting one question each from sections A, B, C and D. Section-E is compulsory.

(ii) All parts of a question should be answered at one place.

(iii) Answers should be brief and to-the-point and be supplemented with neat sketches.

## SECTION - A

1. (a) Explain all the factors that are to be taken into account in order to grow a single crystal of doped silicon by Czochralski technique which is relatively free from point defect, stress, dislocations and with a predecided crystal orientation.

   (b) Describe floatzone technique to grow single crystal silicon. List the steps involved in obtaining Si wafer from Si crystal. (12+8=20)

2. (a) Explain the deposition of silicon nitrite using low pressure chemical vapor deposition technique and plasma enhanced chemical vapor deposition. Compare the properties of silicon nitrite material grown by LPCVD and PECVD process.

   (b) Write notes on DC sputtering and MOCVD. (10+10=20)





## SECTION - B

3. (a) How does Silicon oxidation take place? Explain the kinetics involved in it. What are the advantages of thermal oxidation?

   (b) With a schematic diagram, explain with Molecular Beam Epitaxy growth chamber and the growth process. What are the requirements for good quality epitaxial films? (10+10=20)

4. Describe the dopant addition using diffusion process. Analyze diffusion process using Fick's equation. Compare various mechanisms of dopant addition in semiconductor. (20)

## SECTION - C

5. (a) Explain the stopping mechanism in ion-implantation. Briefly explain the models used for estimating the depth distribution of implanted ions. Explain how annealing repairs the lattice damage and make dopant electrically active.

   (b) What are the major requirements that a resist must satisfy to be useful for submicron technology? Explain e-beam lithography technique for pattern writing. (10+10=20)

6. (a) Explain the process of plasma assisted etching in detail. Explain the anisotropy in plasma etch process and the resulting profile. Explain the effects of plasma parameter on etch rate.

   (b) What are various parameters associated with lithography? Explain the process of photolithography. (8+12=20)

## SECTION - D

7. (a) Explain the sequence of steps in the CMOS fabrication.

(b) Describe the following process steps for fabricating ideal NMOS IC:

(i) Choice of starting material.

(ii) Isolation.

(iii) Channel doping.

(iv) Gate material, and

(v) Source/Drain formation. (10+10=20)

8. (a) What are the limitations of pure aluminum metallization for sub-micron level devices? Explain the method of copper metallization for integrated circuits.

(b) What is BiCMOS technology and explain in detail the basic processing steps involved in BiCMOS process? (10+10=20)

## SECTION - E

9. Answer the following :

(a) What is a clean room? List out different contaminants type and their impact on IC.

(b) Compare direct and contact printing process.

(c) How is anisotropic etching useful in designing feature size?

(d) Why positive resist is preferred over negative resist?

(e) What are the methods to remove oxygen from the active region of the wafer?

(f) What are different isolation techniques used in integrated circuits?

(g) Show that to grow an oxide layer thickness of x, a thickness of .44x of silicon is consumed?

(h) What is twin tub process? Why is it called so?

(i) What are differences between wet and dry etching process?

(j) Explain how etching of gold is done. (2x10=20)